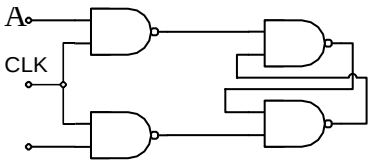
Gate Questions
Dronacharya College of Engineering, Gurgoan

Subject : Digital Electronics

1. Consider the given circuit.



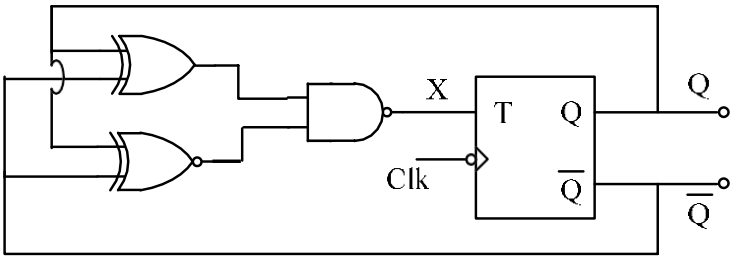
In this circuit, the race around

(A) does not occur (B) occurs when CLK = 0
(C) occurs when CLK = 1 and A = B = 1 (D) occurs when CLK = 1 and A = B = 0

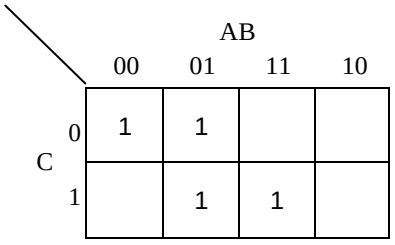
2. A bulb in a staircase has two switches, one switch being at the ground floor and the other one at the first floor. The bulb can be turned ON and also can be turned OFF by any one of the switches irrespective of the state of the other switch. The logic of switching of the bulb resembles

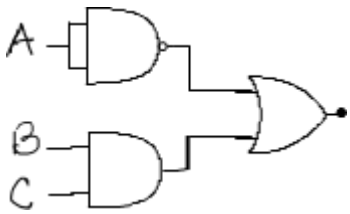
i. an AND gate (B) an OR gate (C) an XOR gate (D) a NAND gate

3. The clock frequency applied to the digital circuit shown in the figure below is 1 kHz. If the initial state of the output Q of the flip- flop is '0', then the frequency of the output waveform Q in kHz is

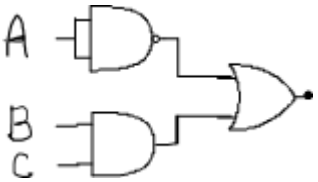


4. Which of the following logic circuits is a realization of the function F whose Karnaugh map is shown in figure

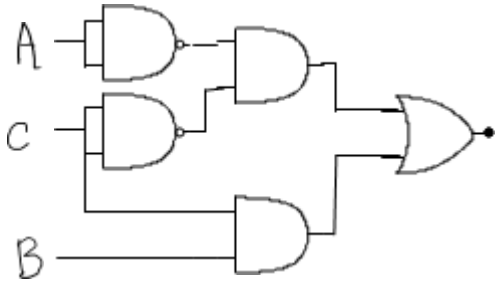




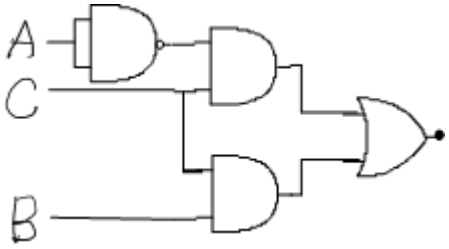
(A)



(B)

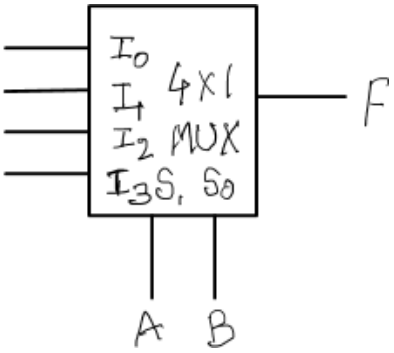


(C)



(D)

5. In the 4×1 multiplexer, the output F is given by $F = A \oplus B$. Find the required input '$I_3I_2I_1I_0$'.



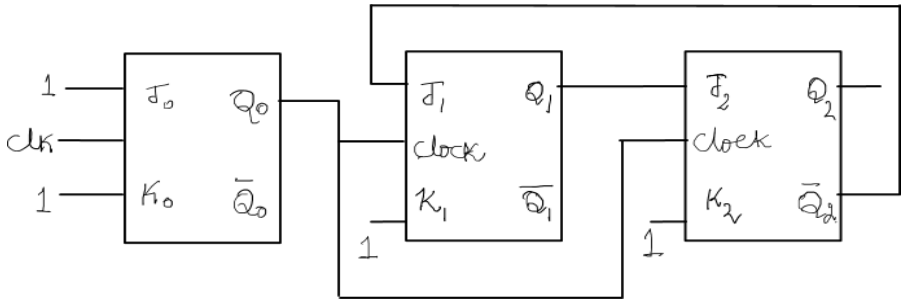
(A) 1010 (B) 0110 (C) 1000 (D) 1110

6.

$ff(A, B, C, D) = \Pi MM(0,1,3,4,5,7,9,11,12,13,14,15)$ is a maxterm representation of a Boolean function $ff(A, B, C, D)$ where A is the MSB and D is the LSB. The equivalent minimized representation of this function is

(A) $(A + \bar{C} + D)(\bar{A} + B + D)$
(B) $A\bar{C}D + \bar{A}BD$
(C) $A\bar{C}D + A\bar{B}CD + AB\bar{C}D$
(D) $(+ \bar{C} + D)(A + B + \bar{C} + D)(\bar{A} + B + C + D)$

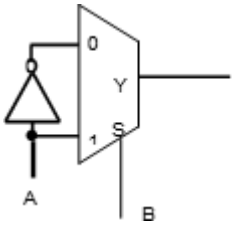
7. The figure shows a digital circuit constructed using negative edge triggered J-K flip flops. Assume a starting state of $Q_2Q_1Q_0$=000. This state $Q_2Q_1Q_0$=000 will repeat after _____ number of cycles of the clock CLK.



8. An 8-bit, unipolar Successive Approximation Register type ADC is used to convert 3.5 V to digital equivalent output. The reference voltage is +5 V. The output of the ADC, at the end of 3rd clock pulse after the start of conversion, is

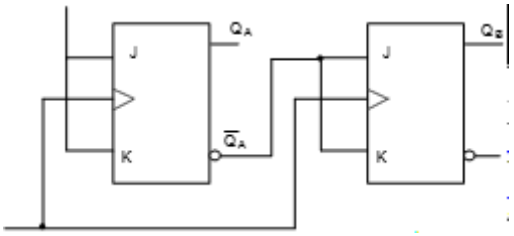
(A) 1010 0000 (B) 1000 0000 (C) 0000 0001 (D) 0000 0011

9. Consider the following circuit which uses a 2-to-1 multiplexer as shown in the figure below. The Boolean expression for output F in terms of A and B is



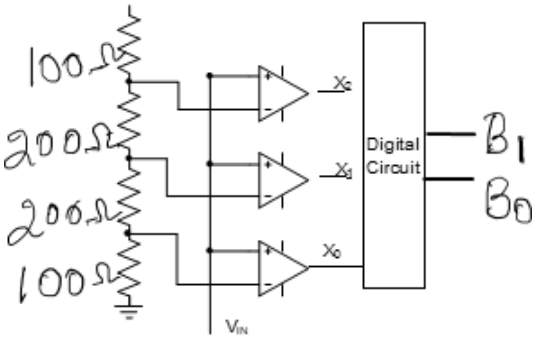
(A) A $\oplus$ B (B) $\overline{A + B}$ (C) $A + B$ (D) $\overline{\text{A} \oplus B}$

10. The current state Q_A Q_B of a two JK flip- flop system is 00. Assume that the clock rise-time is much smaller than the delay of the JK flip-flop. The next state of the systemis



(A) 00 (B) 01 (C) 11 (D) 10

11. A 2-bit flash Analog to Digital Converter (ADC) is given below. The input is $0 \leq V_{IN} \leq 3$ Volts.The expression for the LSB of the output B_0 as a Boolean function of X_2, X_1, and X_0 is



12.12.

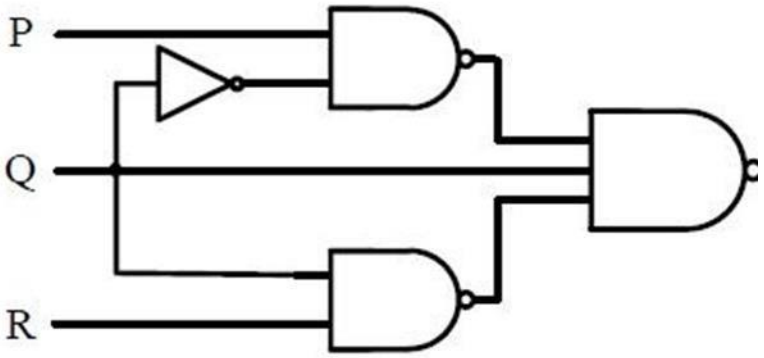
The output expression for the Karnaugh map shown below is

AB \ CD	00	01	11	10
00	0	0	0	0
01	1	0	0	1
11	1	0	1	1
10	0	0	0	0

12. (A) $B\overline{D} + BCD$ (B) $B\overline{D} + AB$
(C) $\overline{B}D + ABC$ (D) $B\overline{D} + ABC$

13.13.

For a 3-input logic circuit shown below, the output Z can be expresse



(A) $Q+\overline{R}$

(B) $P\overline{Q}+R$

(C) $\overline{Q}+R$

(D) $P+\overline{Q}+R$

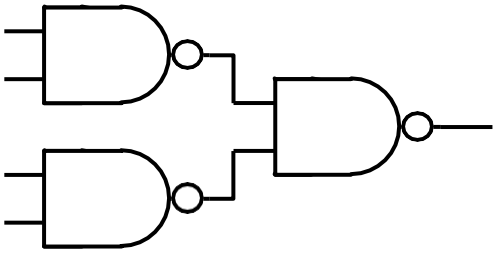
14. In the logic circuit shown in the figure, Y is given by

(A) Y = ABCD

(B) Y = (A + B) (C + D)

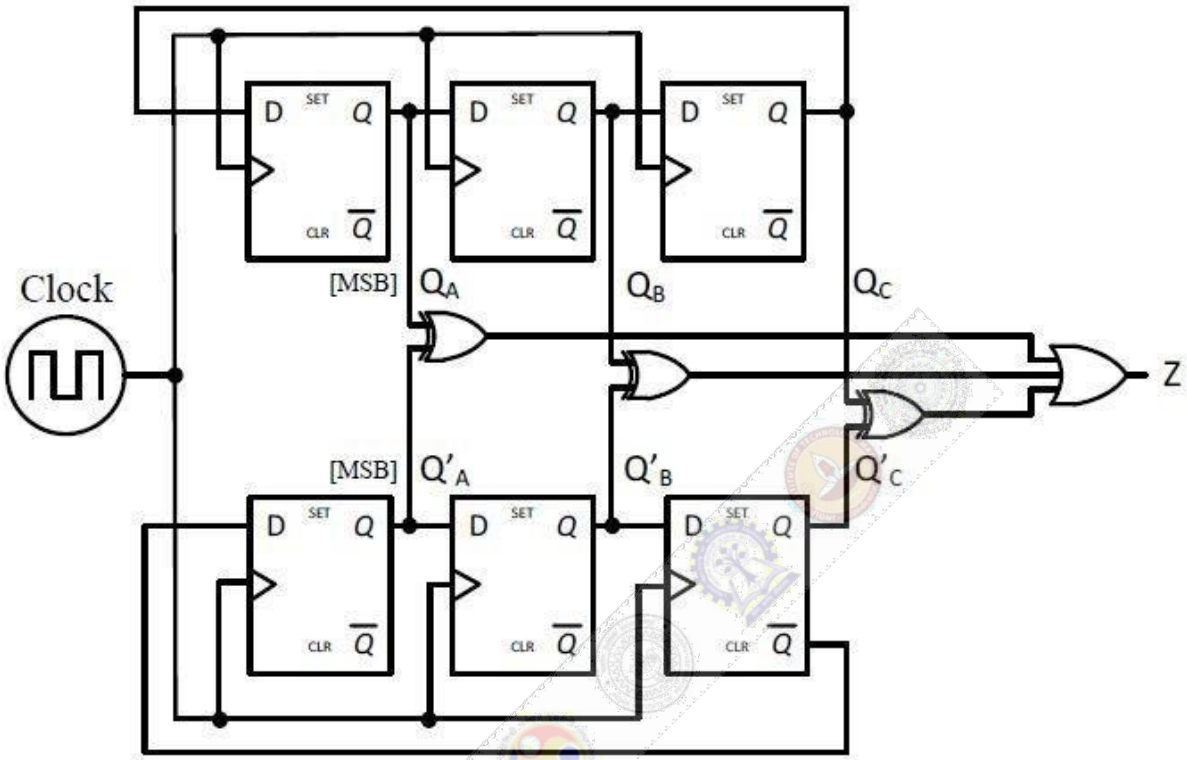
(C) Y = A + B + C + D

(D) Y = AB + CD



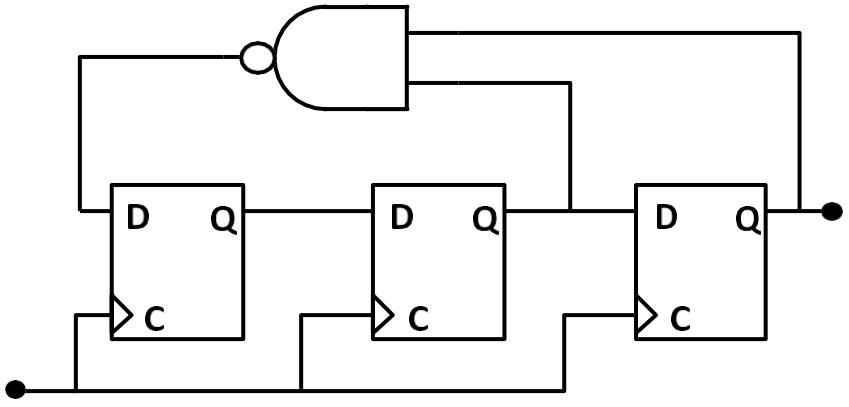
15.15.

For the synchronous sequential circuit shown below, the output Z is zero for the initial conditions $Q_A Q_B Q_C = Q'_A Q'_B Q'_C = 100$.



The minimum number of clock cycles after which the output Z would again become zero is _____

16. Which one of the following statements is true about the digital circuit shown in the figure

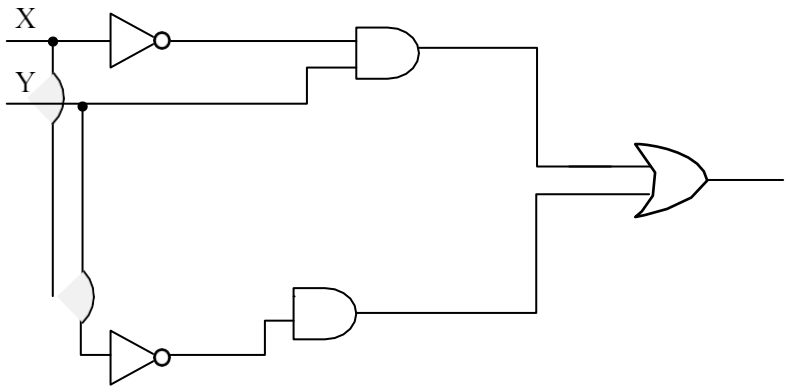


(A) It can be used for dividing the input frequency by 3.
(B) It can be used for dividing the input frequency by 5.
(C) It can be used for dividing the input frequency by 7.
(D) It cannot be reliably used as a frequency divider due to disjoint internal cycles.

17. Digital input signals A, B, C with A as the MSB and C as the LSB are used to realize the Boolean function $F = m_0 + m_2 + m_3 + m_5 + m_7$, where m_i denotes the i^{th} minterm. In addition, F has a don't care for m_1. The simplified expression for F is given by

(A) $\bar{A}\bar{C} + \bar{B}C + AC$ (B) $\bar{A} + C$
(C) $\bar{C} + A$ (D) $A\bar{C} + BC + A\bar{C}$

18. In the circuit shown below, X and Y are digital inputs, and Z is a digital output. The equivalent circuit is a



(A) XOR gate (B) NOR gate (C) XNOR gate (D) NAND gate

19. The output expression for the Karnaugh map shown below is

RS \ PQ	00	01	11	10
00	0	1	1	0
01	1	1	1	1
11	1	1	1	1
10	0	0	0	0

(A) $Q\bar{R} + \bar{S}$ (B) $QR + \bar{S}$ (C) $\bar{Q}R + S$ (D) $QR + S$

20.20. A sequence detector is designed to detect precisely 3 digital inputs, with overlapping sequences detectable. For the sequence (1,0,1) and input data (1,1,0,1,0,0,1,1,0,1,0,1,1,0), what is the output of this detector?

(A) 1,1,0,0,0,0,1,1,0,1,0,0

(B) 0,1,0,0,0,0,0,1,0,1,0,0

(C) 0,1,0,0,0,0,0,1,0,1,1,0

(D) 0,1,0,0,0,0,0,0,1,0,0,0

21. A counter is constructed with three D flip-flops. The input-output pairs are named (D0, Q0), (D1, Q1), and (D2, Q2), where the subscript 0 denotes the least significant bit. The output sequence is desired to be the Gray-code sequence 000, 001, 011, 010, 110, 111, 101, and 100, repeating periodically. Note that the bits are listed in the Q2 Q1 Q0 format. The combinational logic expression for D1 is

(A) $Q_2Q_1Q_0$

(B) $Q_2Q_0 + Q_1\overline{Q_0}$

(C) $\overline{Q_2}Q_0 + Q_1\overline{Q_0}$

(D) $Q_2Q_1 + \overline{Q_2}\overline{Q_1}$